Amendments To The Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

1. (Previously Presented) Apparatus for receiving and processing a CDR signal comprising:

PLD circuitry;

first input circuitry configured to receive the CDR signal, wherein the CDR signal includes data information and a clock signal embedded in a serial data stream;

second input circuitry configured to receive an external reference clock signal, wherein the external reference clock signal has a frequency related to a frequency of the embedded clock signal; and

processing circuitry at least partly controlled by the PLD circuitry and configured to use the external reference clock signal to recover the data information from the CDR signal.

2. (Original) The apparatus defined in claim 1 wherein the PLD circuitry, the first and second input

circuitries, and the processing circuitry are all integrated in a single integrated circuit device.

3. (Original) The apparatus defined in claim 1 wherein the first input circuitry comprises:

phase locked loop circuitry.

4. (Original) The apparatus defined in claim 3 wherein the phase locked loop circuitry is programmable with respect to an operating parameter.

5. (Original) The apparatus defined in claim 3 wherein the phase locked loop circuitry is configured to power down in response to a programmable power down signal.

6. (Original) The apparatus defined in claim 1 wherein the second input circuitry comprises:

phase locked loop circuitry.

7. (Original) The apparatus defined in claim 6 wherein the phase locked loop circuitry is programmable with respect to an operating parameter.

8. (Original) The apparatus defined in claim 6 wherein the phase locked loop circuitry is configured to power down in response to a programmable power down signal.

9. (Original) The apparatus defined in claim 6 wherein the first input circuitry comprises:

further phase locked loop circuitry configured to receive an output signal of the phase locked loop circuitry and to produce a recovered clock signal that is synchronized with the CDR signal.

10. (Original) The apparatus defined in claim 9 wherein the further phase locked loop circuitry is further configured to adjust the phase of the output signal of the phase locked loop circuitry to produce the recovered clock signal.

11. (Original) The apparatus defined in claim 1 wherein the processing circuitry comprises:

deserializer circuitry configured to convert the data information from serial to parallel form.

12. (Original) The apparatus defined in claim 11 wherein the deserializer circuitry is programmable with respect to an operating parameter.

13. (Original) The apparatus defined in claim 11 wherein the deserializer circuitry is further configured to reset in response to a reset signal selectively produced by the PLD circuitry.

14. (Original) The apparatus defined in claim 1 wherein the processing circuitry comprises:

buffer circuitry configured to buffer the data information between a clock regime associated with reference clock signal and a different clock regime.

15. (Original) The apparatus defined in claim 14 wherein the buffer circuitry is further configured to reset in response to a reset signal selectively produced by the PLD circuitry.

16. (Original) The apparatus defined in claim 1 wherein at least one of the first input, second input and processing circuitries is configured to apply to the PLD

circuitry a condition-monitoring signal indicative of an operating condition of that at least one circuitry.

17. (Original) The apparatus defined in claim 1 wherein at least one of the first input, second input, and processing circuitries includes a component that is reset by a reset signal selectively produced by the PLD circuitry.

18. (Original) The apparatus defined in claim 1 wherein the first input circuitry is further configured for alternate use to receive a non-CDR data signal; the second input circuitry is further configured for alternate use to receive a non-CDR clock signal that is synchronized with the non-CDR data signal; and the processing circuitry is further configured for alternate use to derive the data information from the non-CDR data signal using the non-CDR clock signal.

19. (Original) The apparatus defined in claim 18 wherein the non-CDR data signal is an LVDS signal.

20. (Original) The apparatus defined in claim 1 further comprising:

output circuitry configured to receive further data information from the PLD circuitry and to use the

reference clock signal to encode the further data information as a further CDR signal for output by the apparatus.

21. (Original) The apparatus defined in claim 20 further comprising:

loopback circuitry configured to selectively use the further CDR signal as the CDR signal.

22. (Original) The apparatus defined in claim 21 wherein the loopback circuitry is configured so that it can be controlled by a signal from the PLD circuitry.

23. (Original) The apparatus defined in claim 20 further comprising:

loopback circuitry configured to selectively route the CDR signal for output by the apparatus in lieu of the further CDR signal.

24. (Original) The apparatus defined in claim 23 wherein the loopback circuitry is configured so that it can be controlled by a signal from the PLD circuitry.

25. (Original) The circuitry defined in claim 21 wherein the loopback circuitry is further configured for selective control by the PLD circuitry.

26. (Previously Presented) Apparatus for producing and transmitting a CDR signal comprising:

PLD circuitry configured to produce data information and a PLD clock signal;

input circuitry configured to receive an external reference clock signal;

buffer circuitry configured to buffer the data information between a clock regime associated with the PLD clock signal and a different clock regime associated with the external reference clock signal, wherein the clock regimes have different frequencies; and

output circuitry configured to use the reference clock signal to produce the CDR signal including the data information and an embedded clock signal having a frequency related to the external reference clock signal.

27. (Original) The apparatus defined in claim 26 wherein the PLD circuitry, the input circuitry, and the output circuitry are all integrated in a single integrated circuit device.

28. (Original) The apparatus defined in claim 26 wherein the input circuitry comprises:

phase locked loop circuitry.

29. (Original) The apparatus defined in claim 28 wherein the phase locked loop circuitry is programmable with respect to an operating parameter.

30. (Original) The apparatus defined in claim 28 wherein the phase locked loop circuitry is configured to power down in response to a programmable power down signal.

31. (Canceled)

32. (Original) The apparatus defined in claim 26 wherein the output circuitry comprises:

serializer circuitry configured to convert the data information from parallel to serial form.

33. (Original) The apparatus defined in claim 32 wherein the serializer circuitry is programmable with respect to an operating parameter.

34. (Original) The apparatus defined in claim 26 wherein at least one of the input and output circuitries is configured to apply to the PLD circuitry a condition-monitoring signal indicative of an operating condition of that at least one circuitry.

35. (Original) The apparatus defined in claim 26 wherein at least one of the input and output circuitries includes a component that is reset by a reset signal selectively produced by the PLD circuitry.

36. (Original) The apparatus defined in claim 26 wherein the PLD circuitry is further configured to produce a non-CDR clock signal synchronized with the data information, and wherein the output circuitry is further configured for alternative use in outputting the data information in non-CDR form in parallel with the non-CDR clock signal.

37. (Original) The apparatus defined in claim 36 wherein the output circuitry is further configured to selectively frequency-scale the non-CDR clock signal by a predetermined scale factor prior to outputting the non-CDR clock signal in frequency-scaled form.

38. (Original) The apparatus defined in claim 37 wherein the output circuitry is programmable with respect to the scale factor.

39. (Original) The apparatus defined in claim 36 wherein the non-CDR form of the data information is an LVDS signal.

40. (Previously Presented) Apparatus for receiving an information signal which includes data information having clock information for the data information embedded in the data information comprising:

first input circuitry configured to receive the information signal;

circuitry configured to receive a programmable scale factor;

second input circuitry configured to receive an external reference clock signal having a reference frequency which is related to a frequency of the clock information by the programmable scale factor;

reference clock signal processing circuitry configured to use the information signal and the reference clock signal to produce a recovered clock signal having phase

and frequency which respectively correspond to a phase and a frequency of the clock information; and

data recovery circuitry configured to use the recovered clock signal and the information signal to produce a data output signal indicative of the data information in the information signal.

41. (Canceled)

42. (Original) The apparatus defined in claim 40 further comprising:

deserializer circuitry configured to convert the data output signal to a plurality of parallel data subsignals, each of which represents a respective portion of the data information indicated by the data output signal.

43. (Original) The apparatus defined in claim 42 wherein the deserializer circuitry is programmable with respect to how many parallel data subsignals are produced.

44. (Original) The apparatus defined in claim 40 further comprising:

synchronizer circuitry configured to convert the data output signal to a further data output signal

synchronized with a read control signal which can have phase and frequency substantially unrelated to the phase and frequency of the reference clock signal and the recovered clock signal.

45. (Original) The apparatus defined in claim 44 further comprising:

selection circuitry configured to select as a final data output signal either the data output signal or the further data output signal.

46. (Original) The apparatus defined in claim 40 wherein the reference clock signal processing circuitry is further configured to use the scale factor in producing the recovered clock signal.

47. (Original) The apparatus defined in claim 46 wherein the reference clock signal processing circuitry is programmable with respect to the scale factor.

48. (Original) The apparatus defined in claim 40 wherein the information signal is applied to the first input circuitry as a pair of differential signals, and wherein the first input circuitry comprises differential driver circuitry

configured to use the differential signals to produce a single output signal for further processing by the apparatus.

49. (Original) The apparatus defined in claim 40 wherein the reference clock signal is applied to the second input circuitry as a pair of differential signals, and wherein the second input circuitry comprises differential driver circuitry configured to use the differential signals to produce a single output signal for further processing by the apparatus.

50. (Original) The apparatus defined in claim 40 wherein the reference clock signal processing circuitry comprises:

phase locked loop circuitry configured to use the reference clock signal and the scale factor to produce a plurality of candidate further reference clock signals, each having the frequency of the clock information and having a phase which is different from the phases of all the other candidate further reference clock signals.

51. (Original) The apparatus defined in claim 50 wherein the reference clock signal processing circuitry further comprises:

further phase locked loop circuitry configured to use the information signal and the candidate further reference clock signals to produce the recovered clock signal.

52. (Original) The apparatus defined in claim 51 wherein the further phase locked loop circuitry comprises:

selection circuitry configured to select as the recovered clock signal the one of the candidate reference clock signals having the phase that works best with the phase of the clock information.

53. (Original) The apparatus defined in claim 40 wherein the data recovery circuitry comprises:

register circuitry having a data input terminal to which the information signal is applied and a clock input terminal to which the recovered clock signal is applied, the register circuitry being configured to store and output samples of the signal applied to the data input terminal in synchronism with the signal applied to the clock input terminal.

54. (Original) The apparatus defined in claim 53 wherein the data recovery circuitry further comprises:

buffer memory circuitry configured to store multiple successive signal samples output by the register in synchronism with the recovered clock signal and to output those samples in the same order in response to another separate read clock signal.

55. (Original) The apparatus defined in claim 40 wherein the information signal represents successive words of J serial bits of data, and wherein the data recovery circuitry comprises:

shift register circuitry having a plurality of serially connected stages and configured to shift in successive samples of the information signal in synchronism with the recovered clock signal;

frequency divider circuitry configured to divide the recovered clock signal by J to produce a further reference clock signal; and

unload circuitry configured to unload all stages of the shift register circuitry in parallel word form in synchronism with the further reference clock signal.

56. (Original) The apparatus defined in claim 55 wherein the frequency divider circuitry is programmable with respect to J.

57. (Original) The apparatus defined in claim 55 wherein the data recovery circuitry further comprises:

buffer memory circuitry configured to store multiple successive parallel words from the unload circuitry in synchronism with the still further reference clock signal and to output those parallel words in a same order in response to another separate read clock signal.

58. (Original) The apparatus defined in claim 40 further comprising:

PLD circuitry configured to use the data output signal.

59. (Original) The apparatus defined in claim 58 wherein all of the circuitries are disposed on a single integrated circuit.

60. (Original) The apparatus defined in claim 58 further comprising:

routing circuitry configured to selectively apply a signal indicative of the recovered clock signal to the PLD circuitry.

61. (Original) The apparatus defined in claim 44 further comprising:

PLD circuitry configured to produce the read control signal.

62. (Original) The apparatus defined in claim 61 wherein the PLD circuitry is further configured to use the data output signal.

63. (Original) A signaling system comprising:

the apparatus defined in claim 40;

a first source of the information signal;

a second source of the reference clock signal;

a first connection between the first source and the first input circuitry; and

a second connection between the second source and the second input circuitry.

64. (Original) The system defined in claim 63 wherein the first and second input circuitries are disposed on a common integrated circuit which does not also include the first and second sources.

65. (Original) The apparatus defined in claim 40 wherein the information signal is a clock data recovery signal.

66. (Original) The apparatus defined in claim 40 further comprising:

alternative reference clock signal processing circuitry configured to selectively alternatively produce a further reference clock signal based on the reference clock signal and without regard for the information signal.

67. (Original) A digital processing system comprising:

processing circuitry;

a memory coupled to said processing circuitry; and

apparatus as defined in claim 40 coupled to the processing circuitry and the memory.

68. (Original) A printed circuit board on which is mounted apparatus as defined in claim 40.

69. (Original) The printed circuit board defined in claim 68 further comprising:

a memory mounted on the printed circuit board and coupled to the apparatus.

70. (Original) The printed circuit board defined in claim 68 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the apparatus.

71. (Previously Presented) Apparatus for transmitting an information signal which includes data information having clock information for the data information embedded in the data information comprising:

circuitry configured to receive a programmable scale factor;

input circuitry configured to receive an external reference clock signal having a reference frequency which is related to a frequency of the clock information by the programmable scale factor;

reference clock signal processing circuitry configured to use the external reference clock signal to produce a further reference clock signal having the frequency of the clock information;

data source circuitry configured to produce a data signal indicative of the data information; and

data signal processing circuitry configured to process the data signal in accordance with the further reference clock signal to produce the information signal.

72. (Canceled)

73. (Original) The apparatus defined in claim 71 wherein the data source circuitry is configured to produce the data signal as a plurality of parallel data subsignals, each of which represents a respective portion of the data information, and wherein the data signal processing circuitry comprises:

serializer circuitry configured to convert the plurality of parallel data subsignals to a single serial data signal.

74. (Original) The apparatus defined in claim 73 wherein the serializer circuitry is programmable with respect to how many parallel data subsignals are converted.

75. (Original) The apparatus defined in claim 71 wherein the data signal processing circuitry comprises:

synchronizer circuitry configured to receive the data signal in synchronism with a write control signal

and to subsequently output the data signal in synchronism with the further reference clock signal, wherein the write control signal can have phase and frequency which are substantially unrelated to the phase and frequency of the reference clock signal and the further reference clock signal.

76. (Original) The apparatus defined in claim 75 wherein the data signal processing circuitry further comprises:

selection circuitry configured to allow the data signal to selectively bypass the synchronizer circuitry.

77. (Original) The apparatus defined in claim 71 wherein the reference clock signal processing circuitry is further configured to use the scale factor in producing the further reference clock signal.

78. (Original) The apparatus defined in claim 77 wherein the reference clock signal processing circuitry is programmable with respect to the scale factor.

79. (Original) The apparatus defined in claim 71 wherein the reference clock signal is applied to the input

circuitry as a pair of differential signals, and wherein the input circuitry comprises differential driver circuitry configured to use the differential signals to produce a single output signal for further processing by the apparatus.

80. (Original) The apparatus defined in claim 71 wherein the data signal processing circuitry comprises differential driver circuitry configured to transmit the information signal as a pair of differential signals.

81. (Original) The apparatus defined in claim 71 wherein the reference clock signal processing circuitry comprises:

phase locked loop circuitry configured to use the reference clock signal and the scale factor to produce the further reference clock signal.

82. (Original) The apparatus defined in claim 71 wherein the data signal processing circuitry comprises:

register circuitry having a data input terminal to which the data signal is applied and a clock input terminal to which the further reference clock signal is applied, the register circuitry being configured to store samples of the signal applied to the data input terminal and

to output those samples in synchronism with the signal applied to the clock input terminal.

83. (Original) The apparatus defined in claim 71 wherein the data signal comprises a plurality of parallel data subsignals, each of which is indicative of a portion of the data information, and wherein the data signal processing circuitry comprises:

register circuitry having a plurality of data input terminals to which the data subsignals are respectively applied and a clock input terminal to which the further reference clock signal is applied, the register circuitry being configured to store samples of the signals applied to the data input terminals and to output those samples in series in synchronism with the signal applied to the clock input terminal.

84. (Original) The apparatus defined in claim 83 wherein the data signal processing circuitry further comprises:

buffer memory circuitry configured to store multiple successive samples of each of the data subsignals in response to another separate write clock signal and to output

those samples in the same order in synchronism with the further reference clock signal.

85. (Original) The apparatus defined in claim 83 wherein the plurality of parallel data subsignals comprises J parallel data subsignals, and wherein the register circuitry comprises:

shift register circuitry having a plurality of serially connected stages and configured to shift out contents of those stages in series in synchronism with the further reference clock signal;

frequency divider circuitry configured to divide the further reference clock signal by J to produce a still further reference clock signal; and

load circuitry configured to load, in parallel, all stages of the shift register circuitry with samples of the data subsignals in synchronism with the still further reference clock signal.

86. (Original) The apparatus defined in claim 85 wherein the frequency divider circuitry is programmable with respect to J.

87. (Original) The apparatus defined in claim 85 wherein the register circuitry further comprises:

buffer memory circuitry configured to store multiple successive parallel words of samples of the data subsignals in response to another separate write clock signal and to output those parallel words in a same order in response to the still further reference clock signal.

88. (Original) The apparatus defined in claim 71 wherein the data source circuitry comprises PLD circuitry.

89. (Original) The apparatus defined in claim 88 wherein all of the circuitries are disposed on a single integrated circuit.

90. (Original) The apparatus defined in claim 88 further comprising:

routing circuitry configured to selectively apply a signal indicative of the further reference clock signal to the PLD circuitry.

91. (Original) The apparatus defined in claim 75 further comprising:

PLD circuitry configured to produce the write control signal.

92. (Original) The apparatus defined in claim 91 wherein the PLD circuitry is further configured to include the data source circuitry.

93. (Original) A signaling system comprising:

the apparatus defined in claim 71;

a first source of the reference clock signal;

a second receiver of the information signal;

a first connection between the first source and the input circuitry; and

a second connection between the data signal processing circuitry and the second receiver.

94. (Original) The system defined in claim 93 wherein the input circuitry and the data signal processing circuitry are disposed on a common integrated circuit which does not also include the first source and the second receiver.

95. (Original) The apparatus defined in claim 71 wherein the information signal is a clock data recovery signal.

96. (Original) The apparatus defined in claim 71 further comprising:

alternative reference clock signal source circuitry configured to produce an alternative clock signal;

signal selection circuitry configured to allow the alternative clock signal to be alternatively selectively used by the data processing circuitry as the further reference clock signal; and

output circuitry configured to output the alternative clock signal in parallel with the information signal.

97. (Original) The apparatus defined in claim 96 wherein the data signal processing circuitry comprises first differential driver circuitry configured to transmit the information signal as a first pair of differential signals, and wherein the output circuitry comprises second differential driver circuitry configured to transmit the alternative clock signal as a second pair of differential signals.

98. (Original) A digital processing system comprising:

processing circuitry;

a memory coupled to said processing circuitry; and

apparatus as defined in claim 71 coupled to the processing circuitry and the memory.

99. (Original) A printed circuit board on which is mounted apparatus as defined in claim 71.

100. (Original) The printed circuit board defined in claim 99 further comprising:

a memory mounted on the printed circuit board and coupled to the apparatus.

101. (Original) The printed circuit board defined in claim 99 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the apparatus.

102. (Previously Presented) Programmable serializer circuitry comprising:

control circuitry that receives a programmable number;

input circuitry that receives the programmable number of input signals in parallel; and

output circuitry that produces an output signal that is serially indicative of the programmable number input signals one after another.

103. (Currently Amended) The programmable serializer circuitry defined in claim 102 wherein the output signal is synchronized with a first clock signal having a first clock rate, and wherein the circuitry further comprises:

clock rate divider circuitry that divides the clock rate by a programmable factor to produce a second clock signal for timing passage of information indicative of the input signals in parallel from the input circuitry to the output circuitry.

104. (Currently Amended) The programmable serializer circuitry defined in claim 103 wherein the factor is programmable to equal the programmable number.

105. (Currently Amended) The programmable serializer circuitry defined in claim 102 wherein the input circuitry comprises a predetermined plural quantity of register stages, and wherein the number is programmable to any integer value up to and including the plural quantity.

106. (Currently Amended) The programmable serializer circuitry defined in claim 105 wherein the register stages store the input signals in parallel.

107. (Currently Amended) The programmable serializer circuitry defined in claim 106 wherein the register stages further output in parallel to the output circuitry information indicative of the input signals.

108. (Currently Amended) The programmable serializer circuitry defined in claim 102 wherein the output circuitry comprises a predetermined plural quantity of register stages, and wherein the number is programmable to any integer value up to and including the plural quantity.

109. (Currently Amended) The programmable serializer circuitry defined in claim 108 wherein the

register stages store in parallel information from the input circuitry indicative of the input signals.

110. (Currently Amended) The programmable serializer circuitry defined in claim 109 wherein the output circuitry further outputs information from the registers in a predetermined series one after another.

111. (Previously Presented) A programmable system comprising:

programmable serializer circuitry as defined in claim 102; and

programmable logic circuitry for supplying the input signals.

112. (Previously Presented) Programmable deserializer circuitry comprising:

control circuitry that receives a programmable number;

input circuitry that receives an input signal serially indicative of plural bits of information one after another and stores the programmable number of successive ones of those bits; and

output circuitry that produces the programmable number of output signals in parallel, each of the output signals being indicative of a respective one of the bits stored by the input circuitry.

113. (Currently Amended) The programmable deserializer circuitry defined in claim 112 wherein the input signal is synchronized with a first clock signal having a first clock rate, and wherein the circuitry further comprises:

clock rate divider circuitry that divides the clock rate by a programmable factor to produce a second clock signal for timing the passage of information indicative of the bits stored by the input circuitry in parallel from the input circuitry to the output circuitry.

114. (Currently Amended) The programmable deserializer circuitry defined in claim 113 wherein the factor is programmable to equal the programmable number.

115. (Currently Amended) The programmable deserializer circuitry defined in claim 112 wherein the input circuitry comprises a predetermined plural quantity of

register stages, and wherein the number is programmable to any integer value up to and including the plural quantity.

116. (Currently Amended) The programmable deserializer circuitry defined in claim 115 wherein each of the register stages stores one of the bits.

117. (Currently Amended) The programmable deserializer circuitry defined in claim 116 wherein the register stages further output in parallel to the output circuitry information indicative of the bits stored in the register stages.

118. (Currently Amended) The programmable deserializer circuitry defined in claim 112 wherein the output circuitry comprises a predetermined plural quantity of register stages, and wherein the number is programmable to any integer value up to and including the plural quantity.

119. (Currently Amended) The programmable deserializer circuitry defined in claim 118 wherein the register stages store in parallel information from the input circuitry indicative of the bits stored by the input circuitry.

120. (Currently Amended) The programmable deserializer circuitry defined in claim 119 wherein the output circuitry further outputs information from the registers in parallel.

121. (Previously Presented) A programmable system comprising:

programmable deserializer circuitry as defined in claim 112; and

programmable logic circuitry for receiving the output signals.

122. (Previously Presented) Apparatus for receiving and processing a plurality of CDR signals, each of which includes data information and clock information, comprising:

first circuitry producing a plurality of candidate recovered clock signals from a reference clock signal, the candidate recovered clock signals having phases that are shifted relative to one another; and

a plurality of second circuitries, each receiving a respective one of the CDR signals and using the candidate reference clock signals to recover the clock

information from the CDR signal received by that second circuitry.

123. (Previously Presented) The apparatus defined in claim 122 wherein the clock information of all of the CDR signals has a predetermined common frequency.

124. (Previously Presented) The apparatus defined in claim 123 wherein the reference clock signal has frequency having a predetermined relationship to the predetermined common frequency.

125. (Previously Presented) The apparatus defined in claim 124 wherein the first circuitry comprises phase locked loop circuitry.

126. (Previously Presented) The apparatus defined in claim 124 wherein each of the second circuitries comprises:

selection circuitry that selects at least one of the candidate recovered clock signals that is close in phase to the clock information in the CDR signal received by that second circuitry.

127. (Previously Presented) The apparatus defined in claim 124 wherein each of the second circuitries comprises:

selection circuitry that selects one of the candidate recovered clock signals that is closest in phase to the clock information in the CDR signal received by that second circuitry.

128. (Previously Presented) Apparatus for receiving and processing a CDR signal comprising:

first input circuitry operative to receive the CDR signal, wherein the CDR signal includes data information and a clock signal embedded in a serial data stream;

second input circuitry operative to receive a reference clock signal, wherein the reference clock signal has a frequency related to a frequency of the embedded clock signal;

phase locked loop circuitry operative to use the reference clock signal to generate a recovered clock signal having a frequency equal to the frequency of the embedded clock signal; and

processing circuitry operative to use the recovered clock signal to recover the data information from the CDR signal.

129. (Previously Presented) The apparatus defined in claim 128 wherein the first input circuitry, the second input circuitry, the phase locked loop circuitry, and the processing circuitry are all integrated in a single integrated circuit device that includes PLD circuitry.

130. (Previously Presented) The apparatus defined in claim 128 wherein the phase locked loop circuitry is programmable with respect to an operating parameter.

131. (Previously Presented) The apparatus defined in claim 128 wherein the frequency of the reference clock signal is related to the frequency of the embedded clock signal by a scale factor.

132. (Previously Presented) The apparatus defined in claim 128 wherein the phase locked loop circuitry is further operative to adjust the phase of the output signal of the phase locked loop circuitry to produce the recovered clock signal.

133. (Previously Presented) The apparatus defined in claim 128 wherein the processing circuitry comprises:

deserializer circuitry operative to convert the data information from serial to parallel form.

134. (Previously Presented) The apparatus defined in claim 128 further comprising:

output circuitry operative to receive further data information and to use the reference clock signal to encode the further data information as a further CDR signal for output by the apparatus.

135. (Previously Presented) The apparatus defined in claim 134 further comprising:

loopback circuitry operative to selectively use the further CDR signal as the CDR signal.

136. (Previously Presented) The apparatus defined in claim 134 further comprising:

loopback circuitry operative to selectively route the CDR signal for output by the apparatus in lieu of the further CDR signal.

137. (Previously Presented) Apparatus for producing and transmitting a CDR signal comprising:

first input circuitry operative to receive a reference clock signal;

second input circuitry operative to receive a data information signal;

phase locked loop circuitry operative to use the reference clock signal to generate an embedded clock signal;

buffer circuitry operative to buffer the data information between a clock regime associated with the data information and a clock regime associated with the embedded clock signal, wherein the clock regimes have different frequencies; and

output circuitry operative to use the embedded clock signal to produce the CDR signal from the data information signal.

138. (Previously Presented) The apparatus defined in claim 137 wherein the first input circuitry, the second input circuitry, the phase locked loop circuitry, the buffer circuitry, and the output circuitry are all integrated in a single integrated circuit device that includes PLD circuitry.

139. (Previously Presented) The apparatus defined in claim 137 wherein the phase locked loop circuitry is programmable with respect to an operating parameter.

140. (Previously Presented) The apparatus defined in claim 137 wherein the frequency of the reference clock signal is related to the frequency of the embedded clock signal by a scale factor.

141. (Previously Presented) The apparatus defined in claim 137 wherein the output circuitry comprises:

serializer circuitry operative to convert the data information from parallel to serial form.